ABSTRACT

A low loss on-die interconnect structure includes first and second differential signal lines on one of the metal layers of a microelectronic die. One or more traces may also be provided on another metal layer of the die that are non-parallel (e.g., orthogonal) to the differential signal lines. Because the traces are non-parallel, they provide a relatively high impedance return path for signals on the differential signal lines. Thus, a signal return path through the opposite differential line predominates for the signals on the differential lines. In one application, the low loss interconnect structure is used within an on-die salphasic clock distribution network.

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